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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,621	01/20/2004	Stephen Paul Wilcox	104969-50918	8240

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,621	WILCOX ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/760,621 filed on 01/20/2004, claims 1-15 are pending in this office action.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 0301249.9 (United Kingdom), filed on 01/20/2003.

Drawings

3. The drawings were received on 03/01/2004. These drawings are accepted by Examiner.

Claim Objections

4. Claims 1, 3, 4, 7, 8, 10, 14, and 15 are objected to because of the following informalities:

Claims 1, 7, 8, 10, 14, and 15 are cited *"each element", "plurality of elements", and "that element"*, that is unclear what are they? Examiner interprets that the *"element"* cited in these claims as *"clocked state holding element"*. If it is corrected, then they should be revised as "each *clock state holding element", "said/the clock state holding element", and "plurality of state holding element",* respectively.

Claim 3 recites the limitation "*the most efficient function*" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 4, before *"wherein"* replaces *"claim 4"* with *"claim 3"*.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-2, 5-11, and 14 –15 are rejected under 35 U.S.C. 101 because these claims appear as listing an abstract idea of simplifying an input logic gate function of a plurality of clocked state holding elements, but the claims do not result in a physical transformation nor they appear to provide a useful, concrete, and tangible result. See MPEP § 2105.

Therefore, claims 1-2, 5-11, and 14–15 appear non-statutory. It is noticed simplifying an input logic gate function of a plurality of clocked state holding elements by reducing a number of logic gates, which provides the input logic for plurality of clocked state holding elements more efficiency in claims 3 and 4 as exemplary. useful/tangible result in clms 3-4 PD

Claim 9 is directly to non-statutory because the claimed invention appears of listing computer software without storing into computer-readable medium and executing by a computer or processor to perform the method as cited in claim 1. Therefore, listing computer software is functional material, which is non-statutory. See MPEP § 2105.

Other dependent claims, which are not specifically cited above, are also rejected because the based claims have been rejected.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 10, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps. See MPEP § 2172.01. The omitted steps are: how to determining a common gating function in order to using the common gating function to implement the second Boolean function for inputting the respective clock state holding element. In order to resolved this issue, Examiner suggests that the limitations cite in claim 7 should be incorporated into claim 1 as exemplary.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1–15 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (hereinafter as "Wu") (Clock-gating and Its Application to Low Power Design of Sequential Circuits, March 2000, IEEE, Vo. 47,Pages 415-419).

10. With respect to claims 1, 10, and 15, Wu discloses a method, apparatus, computer system of determining an input function for each of a plurality of clocked state holding elements *(sequential circuit) (the abstract and figures 3 and 4)*, said method comprising the steps of:

(means for) determining, for each element, a first Boolean function corresponding to variables forming an input to that element *(figures 3(a) and 3(b), each flip-flop has gate(s) is a first Boolean function input to each flip-flop and see whole article)*;

(means for) determining a common gating function for the plurality of elements *(figure 2, finding a common gate of using Karnaugh map and see whole article)*; and

(means for) determining, for each element, a second Boolean function based on the first Boolean function and the common gating function *(figure 2, finding a common gate of using Karnaugh map and group value "1" and don't care to simplify a input circuit to implement second Boolean function and see whole article)*, each said second Boolean function being determined such that it provides the same result as the respective first Boolean function when the common gating function has a value of 1 *(figure 2, finding a common gate of using Karnaugh map and group value "1" and don't care to simplify a input circuit as figures 4(a) and 4(b))*, wherein each second Boolean function forms an input function for the respective element *(figures 4(a) and 4(b) is the second Boolean function as simpler to compare to first input circuit as figures 3(a) and 3(b) and see whole article).*

11. With respect to claims 2 and 11, Wu discloses all the limitations at set forth claims, further comprising the step of selectively replacing each said first Boolean function with its respective second Boolean function *(replaces Di= Not (Qi) as figures 4(a) and 4(b) with input circuits as D1, D2, D3 as figures 3(a) and 3(b) and see whole article).*

12. With respect to claims 3 and 12, Wu discloses all the limitations at set forth claims, wherein said step of selectively replacing is dependent upon a comparison of each first and respective second Boolean function to determine which is the most efficient function *(experiment result show that these design have ideal logic functionality*

(efficient function) with lower power distribution compared to traditional designs) (the abstract and figures 4(a) and 4(b) is simpler than figures 3(a) and 3(b), respectively. There is power saving since the four flip-flop are isolated from the triggering clock in the idle cycles and see whole article).

13. With respect to claims 4 and 13, Wu discloses all the limitations at set forth claims, wherein the most efficient function is the one that can be implemented with a smaller number of implementation in terms of logical gates *(number logic gates as input logic of figures 4(a) and 4(b) is less than figures 3(a) and 3(b), respectively and see whole article).*

14. With respect to claim 5, Wu discloses the method according to claim 1, wherein the second Boolean function is created by applying an algorithm to the first Boolean function *(table I and figures 2-4 and see whole article).*

15. With respect to claim 6, Wu discloses the method according to claim 5, wherein the algorithm creates a Karnaugh map *(figures 2(a), 2(b), and 2(c) and see whole article).*

16. With respect to claims 7 and 14, Wu discloses all the limitations at set forth claims, wherein the elements have at least one common input and the gating function is determined by the steps of: determining, for each element, the conditions under which that element will hold its current value based only on the common inputs *(table I, holding state as "0" and "1" and see whole article)*; and combining, for each element, the determined conditions to form the gating function for that element *(figure 2(c), combining all holding value "1" and "don't care" and see whole article).*

17. With respect to claim 8, Wu discloses the method according to claim 1, wherein the Boolean function for each element determines the conditions under which the element will hold its current value *(figure 2(c), combining all holding value "1" and "don't care" and see whole article)*.

18. With respect to claim 9, Wu discloses the method according to claim 1, wherein the recited steps are carried out by computer software *(the rejection is applied as claim 1)*.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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